蔚華科技 SPIROX

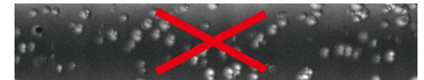
SOUTHPORT

Southport Corporation
南方科技股份有限公司

JadeSiC-NK Non-Destructive Inspection System for SiC Crystal Killer-Defects Detection

The Best Substitution for KOH Etching Method

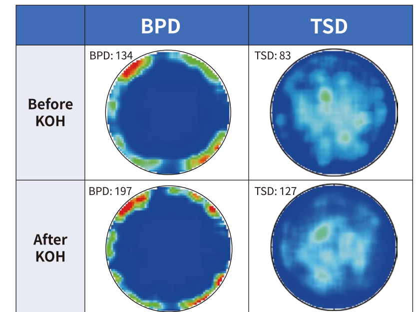
- Industry first technology for non-destructive defect inspection for SiC substrates
- Direct insight to SiC substrates wafer mapping for killer defects distribution
- Effective monitor the quality of SiC substrates
- Significant costs reduction comparing to KOH etching by avoid etching SiC substrates



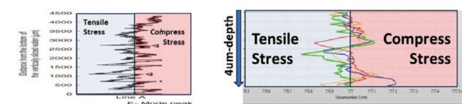
No more costly KOH etching process

Features

- Detect and identify defects on the surface and inside of SiC substrates with advanced NLO (non-linear optics) technology.
- Non-destructive inspection to replace costly KOH etching method.
- Whole SiC wafer defect scanning ability provides more accurate defect density distribution over the sampling interpolation of KOH etching method.
- Focus on the most killing defects (BPD, TSD, MP, SF) detection for SiC substrates.
- Support 2”, 4”, 6”, 8” SiC substrates inspection.
- Optional function of MicroArea 3D scan available.



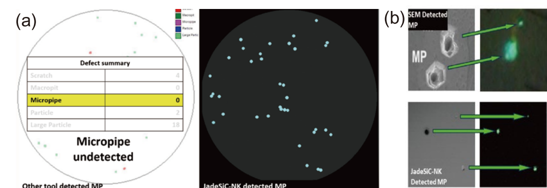
Comparison of BPD/TSD density distribution before (by JadeSiC-NK) and after KOH etching



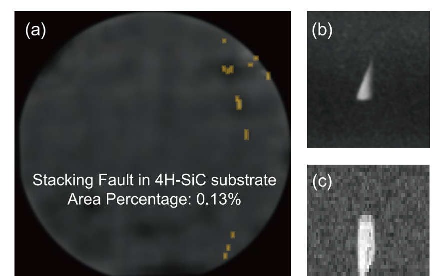
Raman Spectrum analysis verified BPD detected by JadeSiC-NK

Advantages

- Effective inspection and analysis tool to improve wafer process yield and significantly reduce direct and indirect production costs.
- No costly SiC substrate wasted, free of toxic, corrosive and hazardous material.
- JadeSiC-NK performs whole wafer scanning to more accurately present killer defect density distribution, as opposed to using traditional optical image sampling interpolation.
- The best tool for continuous production process improvement.



(a) MicroPipes detected by JadeSiC-NK and other existing technology.
(b) PL Spectrum analysis verified Micropipes detected by JadeSiC-NK.



(a) SF (Stacking Fault) detected by JadeSiC-NK
(b)-(c) The images of Stacking Faults.

Benefits

- Effectively and reliably detect and identify killer crystal defects of SiC.
- Significantly reduce direct and indirect costs, which transfer to increase SiC substrate output compared to KOH etching method
- State-of-the-art tool for SiC substrate production process improvement
  → Low-cost DOE (Design Of Experiment)
  → 100% inspection on extracted substrates out of one ingot for detailed ingot level quality analysis.
  → Enable effective tracking and analyzing ingots made by different batch or furnace.

Specifications

Model Number	SP3055A	
Model Name	JadeSiC-NK, non-destructive inspection system for SiC killer defects (BPD, TSD, MP, SF), the best substitution for KOH etching method.	
SiC Substrate / EPI Wafer Size	2” 4” 6” 8”	
Wafer Thickness	300 μm - 550 μm	
Chuck	XY Stage Repeatability : 0.1 μm	
Inspection Items	Whole Wafer Defect Scan (MicroPipe, BPD, TED, TSD, Stacking Fault, etc.)	
Whole Wafer Defect Scan	Estimated Inspection Time	1 hr @4” wafer 2 hrs @6” wafer 4 hrs @8” wafer
	Lateral Resolution	1 μm
	Analysis	MicroPipe Density (MPD) BPD/TED/TSD Density Stacking Fault Area Percentage Wafer Yield Tri-angle and Carrot**
MicroArea 3D Scan (optional)	Field of View	400 μm x 400 μm
	Scanning Zoom	Yes (1x - 10x)
	Scan Resolution	Up to 1024 x 1024
	Lateral Resolution	0.4 μm
	Axial Resolution	0.25 μm
	Min. Increment of Z stage	0.02 μm
	Wide Field Module Camera	Color Camera (FOV 400 μm x 400 μm)

* : can be extended to SiC epi ** : Epi defect

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